NVIDIA Tesla GPU - Power Brake

```
nvidia-smi -q | grep HW
        HW Slowdown                 : Active
            HW Thermal Slowdown         : Not Active
            HW Power Brake Slowdown     : Active
```

Your server vendor may block GPUs not on a HCL. HW Power Brake Slowdown on NVIDIA Tesla GPUs is documented with a fixed slowdown of 50% in performance and power limit (see Data Sheet).

You can prevent the system from activating the "HW Power Brake" by blocking PCIe Pin B30. Pin B30 has been a reserved pin for long time. This has changed to Pin B30 being a PWRBRK for emergency power reduction.

Emergency Power Reduction Mechanism with PWRBRK Signal ECN This ECN defines two sets of related changes to support an Emergency Power Reduction mechanism and to provide software visibility for this mechanism: 1. The Card Electromechanical Specification is updated to define an optional Emergency Power Reduction mechanism using RSVD pin B30. 2. The PCI Express Base Specification is updated to define an optional mechanism to indicate support for Emergency Power Reduction and to provide visibility as to the power reduction status of a Device. show less	3.x	ECN	**December 1, 2015**

Source: https://pcisig.com/specifications/pciexpress/

Tape or use a waterproof marker to block Pin B30. B30 is on the cooler side 30th Pin.

```
nvidia-smi -q | grep HW
        HW Slowdown                 : Not Active
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```

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power & Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset [23]
Key notch			
12	CLKREQ#[24]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			
19	HSOp(1)	Reserved	Lane 1 transmit data, + and −
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and −
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and −
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and −
30	PWRBRK#[25]	HSIn(3)	"Power brake", active-low to reduce device power
31	PRSNT2#	Ground	
32	Ground	Reserved	

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